CLAIMS:

1. An Analog-to-Digital-Converter (ADC) that receives an analog signal and that converts the analog signal to digital data, the ADC comprising:

a modulator that receives the analog signal and a feedback signal, wherein the modulator modulates the analog signal to produce a modulated signal at a modulator clock rate;

a decimation filter coupled to the modulator to receive the modulated signal, wherein the decimation filter decimates and filters the modulated signal to produce the digital data; and

a time dither clock reduction circuit that receives the modulated signal and that provides the feedback signal to the modulator, wherein the time dither clock reduction circuit applies both clock reduction and time dithering to the modulated signal to produce the feedback signal.

2. The ADC of claim 1, wherein:

at each modulator clock cycle, the time dithering clock reduction circuit considers modulated signals for a dithering factor, N, previous modulator clock cycles and a modulated signal for a current modulator clock cycle; and

if at least one constraint is satisfied for the N previous modulator clock cycles, the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal.

3. The ADC of claim 2, wherein if the prior feedback signal is one, a sum of the modulated signals for the N previous modulator clocks is equal to N, and the modulated signal for the current modulator clock is zero, the time dithering clock reduction circuit transitions the feedback signal from one to zero.

4. The ADC of claim 2, wherein if the prior feedback signal is one, a sum of the modulated signals for the N previous modulator clocks is equal to N, and the modulated signal for the current modulator clock is one, the time dithering clock reduction circuit holds the feedback signal at one.

5. The ADC of claim 2, wherein if the prior feedback signal is zero, a sum of the modulated signals for the N previous modulator clocks is equal to zero, and the modulated signal for the current modulator clock is one, the time dithering clock reduction circuit transitions the feedback signal from zero to one.

6. The ADC of claim 2, wherein if the prior feedback signal is zero, a sum of the modulated signals for the N previous modulator clocks is equal to zero, and the modulated signal for the current modulator clock is zero, the time dithering clock reduction circuit holds the feedback signal at zero.

7. The ADC of claim 2, wherein after the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal, a new dithering factor, N, is selected.

8. The ADC of claim 7, wherein the new dithering factor is determined by:

generating a random number; and

the new dithering factor is based upon a comparison of the random number to at least one constraint.

9. The ADC of claim 1, wherein:

the modulator comprises an analog delta sigma block having an integrator and a quantizer;

the integrator receives the analog signal and the feedback signal and produces an integrator output; and

the quantizer receives the integrator output and produces the modulated signal.

10. The ADC of claim 9, wherein the quantizer is a two level quantizer.

11. The ADC of claim 9, wherein the quantizer is a three level quantizer.

12. The ADC of claim 1, wherein:

the modulated signal includes at least three levels including -1, 0, and 1;

at each modulator clock cycle, the time dithering clock reduction circuit considers modulated signals for a dithering factor, N, previous modulator clock cycles and a modulated signal for a current modulator clock cycle; and

if at least one constraint is satisfied for the N previous modulator clock cycles, the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal.

13. The ADC of claim 12, wherein if the absolute value of the prior feedback signal is one and the absolute value of a sum of the modulated signals for the N previous modulator clocks is equal to N, the time dithering clock reduction circuit allows the feedback signal to transition with the modulated signal.

14. The ADC of claim 12, wherein if the absolute value of the prior feedback signal is one and the absolute value of a sum of the modulated signals for the N previous modulator clocks is not equal to N, the time dithering clock reduction circuit holds the feedback signal.

15. The ADC of claim 12, wherein if the absolute value of the prior feedback signal is not equal to one and the sum of the modulated signals for the N previous modulator clocks is equal to zero, the time dithering clock reduction circuit allows the feedback signal to transition with the modulated signal.

16. The ADC of claim 12, wherein if the absolute value of the prior feedback signal is not equal to one and the sum of the modulated signals for the N previous modulator clocks is not equal to zero, the time dithering clock reduction circuit holds the feedback signal.

17. The ADC of claim 12, wherein after the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal, a new dithering factor, N, is selected.

18. The ADC of claim 1, wherein the decimation filter includes:

at least one integrator stage;

at least one differentiator stage; and

at least one decimation stage.

19. The ADC of claim 1, wherein the time dither clock reduction circuit includes time dither clock reduction logic and a dithering factor generator.

20. A Wireless Local Area Network (WLAN) transceiving integrated circuit that services voice communications in a WLAN with at least one WLAN device, the WLAN transceiving integrated circuit comprising:

a WLAN interface that wirelessly communicates with the at least one WLAN device to receive inbound packetized audio data from the at least one WLAN device and to transmit outbound packetized audio data to the at least one WLAN device;

a transcoder operably coupled to the WLAN interface, wherein the transcoder receives the inbound packetized audio data and converts the inbound packetized audio data to inbound Pulse Code Modulated (PCM) WLAN audio data, and wherein the transcoder receives outbound PCM WLAN audio data and converts the outbound PCM WLAN audio data to the outbound packetized audio data; and

an audio coder/decoder operably coupled to the transcoder that produces the outbound PCM WLAN audio data, the coder/decoder including an analog to digital converter that receives an analog audio signal and that converts the analog audio signal to PCM WLAN audio data, the analog to digital converter including:

a modulator that receives the analog audio signal and a feedback signal, wherein the modulator modulates the analog audio signal to produce a modulated signal at a modulator clock rate;

a decimation filter coupled to the modulator to receive the modulated signal, wherein the decimation filter decimates and filters the modulated signal to produce the PCM WLAN audio data; and

a time dither clock reduction circuit that receives the modulated signal and that provides the feedback signal to the modulator, wherein the time dither clock reduction

circuit applies both clock reduction and time dithering to the modulated signal to produce the feedback signal.

21. The WLAN transceiving integrated circuit of claim 20, wherein:

at each modulator clock cycle, the time dithering clock reduction circuit considers modulated signals for a dithering factor, N, previous modulator clock cycles and a modulated signal for a current modulator clock cycle; and

if at least one constraint is satisfied for the N previous modulator clock cycles, the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal.

22. The WLAN transceiving integrated circuit of claim 21, wherein if the prior feedback signal is one, a sum of the modulated signals for the N previous modulator clocks is equal to N, and the modulated signal for the current modulator clock is zero, the time dithering clock reduction circuit transitions the feedback signal from one to zero.

23. The WLAN transceiving integrated circuit of claim 21, wherein if the prior feedback signal is one, a sum of the modulated signals for the N previous modulator clocks is equal to N, and the modulated signal for the current modulator clock is one, the time dithering clock reduction circuit holds the feedback signal at one.

24. The WLAN transceiving integrated circuit of claim 21, wherein if the prior feedback signal is zero, a sum of the modulated signals for the N previous modulator

clocks is equal to zero, and the modulated signal for the current modulator clock is one, the time dithering clock reduction circuit transitions the feedback signal from zero to one.

25. The WLAN transceiving integrated circuit of claim 21, wherein if the prior feedback signal is zero, a sum of the modulated signals for the N previous modulator clocks is equal to zero, and the modulated signal for the current modulator clock is zero, the time dithering clock reduction circuit holds the feedback signal at zero.

26. The WLAN transceiving integrated circuit of claim 21, wherein after the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal, a new dithering factor, N, is selected.

27. A method for converting an analog signal to digital data comprising:

modulating the analog signal based upon a feedback signal to produce a modulated signal at a modulator clock rate;

decimating and filtering the modulated signal to produce the digital data; and

applying both clock reduction and time dithering to the modulated signal to produce the feedback signal based upon the modulated signal.

28. The method of claim 27, further comprising:

at each modulator clock cycle, considering modulated signals for a dithering factor, N, previous modulator clock cycles and a modulated signal for a current modulator clock cycle; and

if at least one constraint is satisfied for the N previous modulator clock cycles, allowing the feedback signal to transition with the modulated signal.

29. The method of claim 28, wherein if the prior feedback signal is one, a sum of the modulated signals for the N previous modulator clocks is equal to N, and the modulated signal for the current modulator clock is zero, the feedback signal transitions from one to zero.

30. The method of claim 28, wherein if the prior feedback signal is one, a sum of the modulated signals for the N previous modulator clocks is equal to N, and the modulated signal for the current modulator clock is one, the feedback signal is held at one.

31. The method of claim 28, wherein if the prior feedback signal is zero, a sum of the modulated signals for the N previous modulator clocks is equal to zero, and the modulated signal for the current modulator clock is one, the feedback signal transitions from zero to one.

32. The method of claim 28, wherein if the prior feedback signal is zero, a sum of the modulated signals for the N previous modulator clocks is equal to zero, and the modulated signal for the current modulator clock is zero, the feedback signal is held at zero.

33. The method of claim 28, wherein after the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal, a new dithering factor, N, is selected.

34. The method of claim 33, wherein the new dithering factor is determined by:

generating a random number; and

basing the new dithering factor upon a comparison of the random number to at least one constraint.